Considerations for Implementing a Zone-Selective Interlocking Scheme on Medium and Low Voltage Systems

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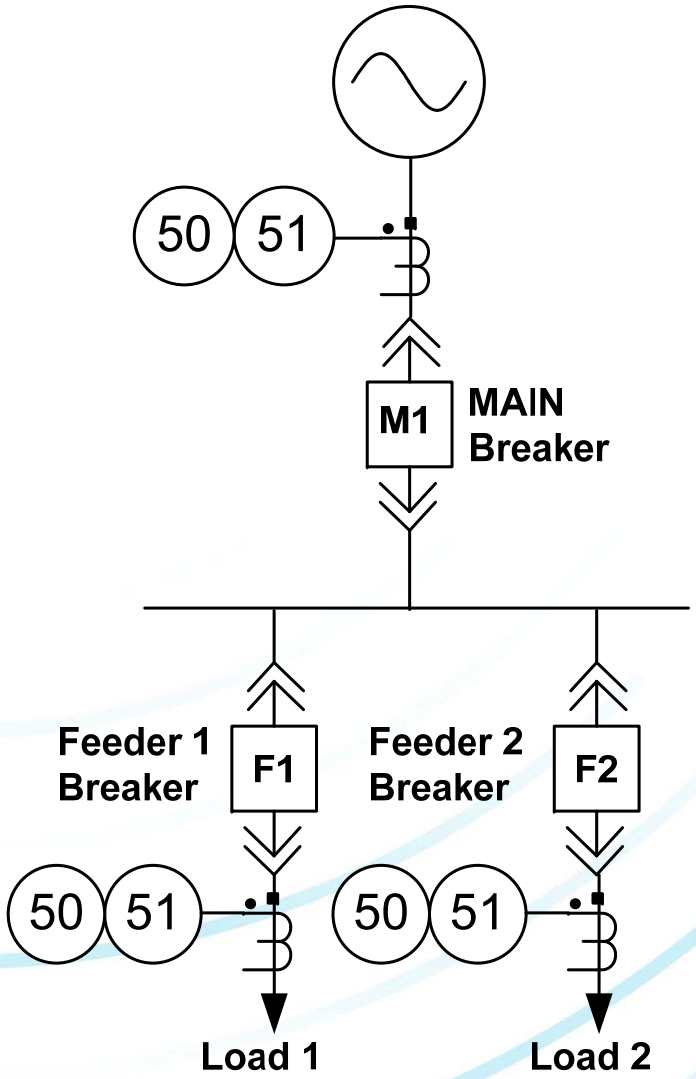
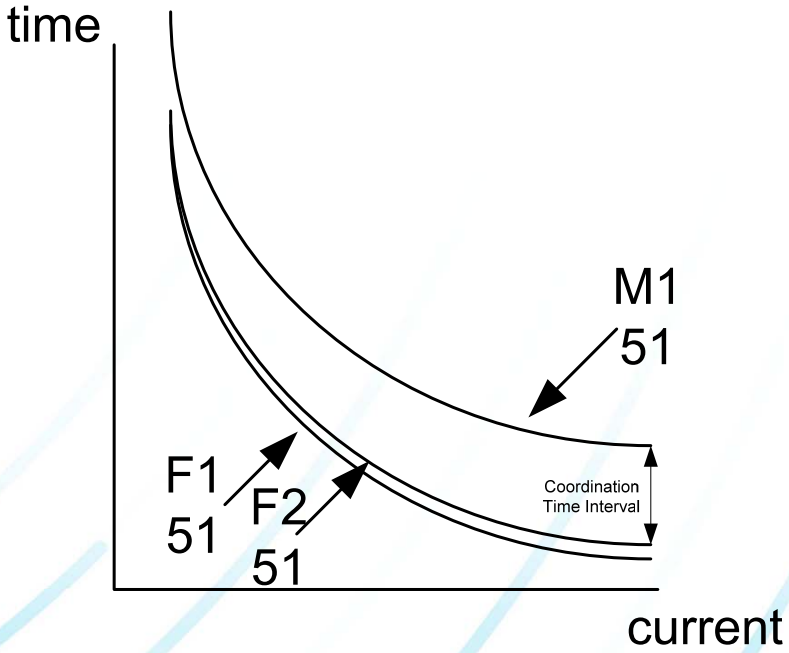
2017 MIPSYCON

Zone-Selective Interlocking

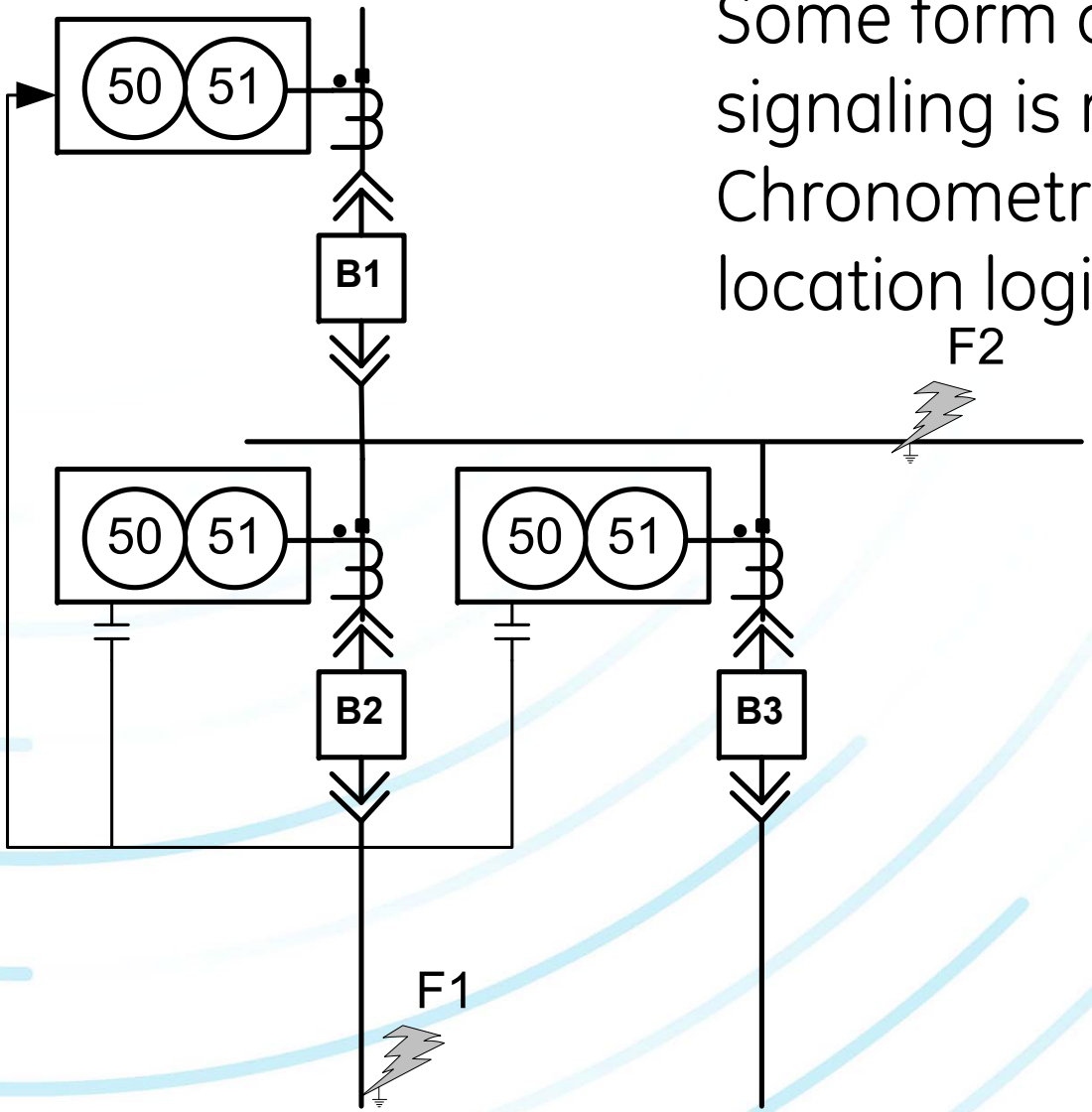


Used when time-overcurrent delay is unacceptable.

"Chronometric coordination"

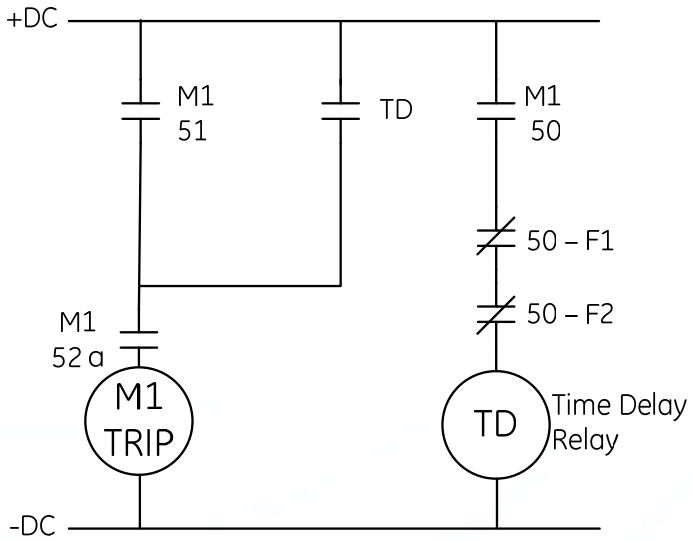


Zone-Selective Interlocking



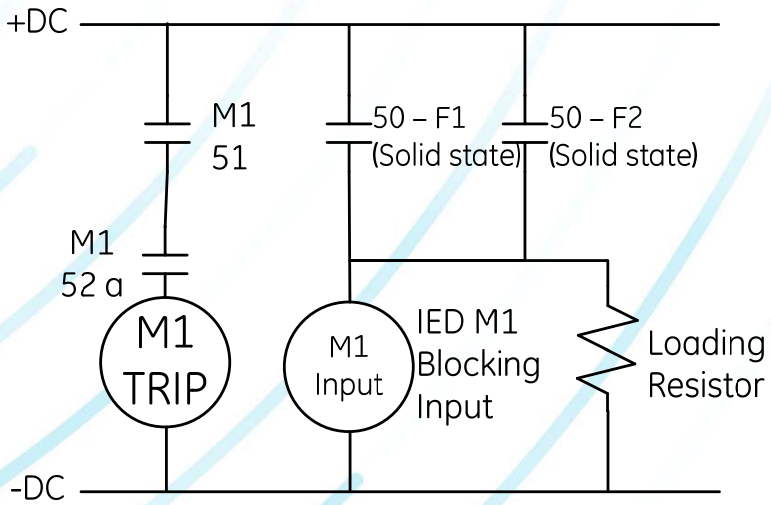
Some form of Inter-IED signaling is required. Chronometric coordination + location logic.

Zone-Selective Interlocking - Hardwiring



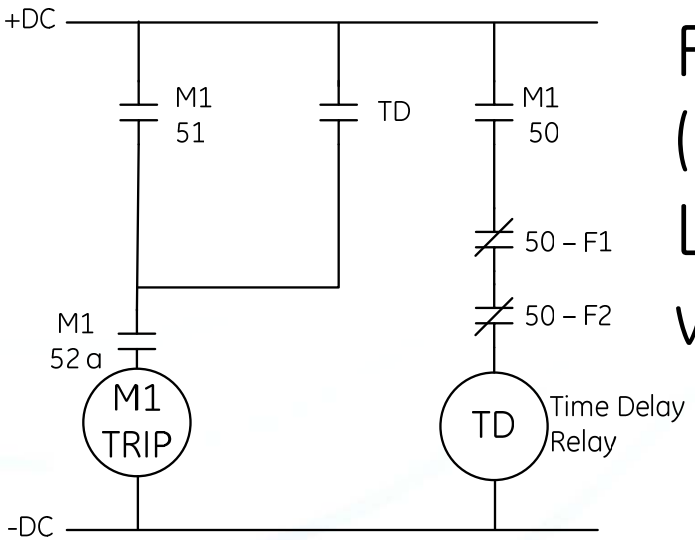
Mechanical relay contacts can take approximately 4 ms to 10 ms to operate.

Solid-state contacts can take approximately 0.1 ms to operate but have leakage current. Beware false-positives!



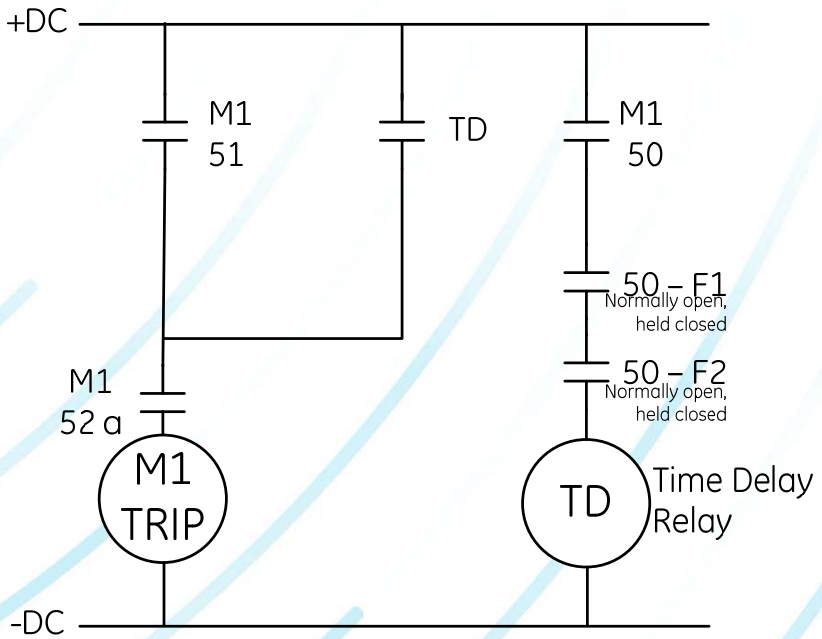
Zone-Selective Interlocking - Hardwiring

Implemented in relays, failure mode is selectable

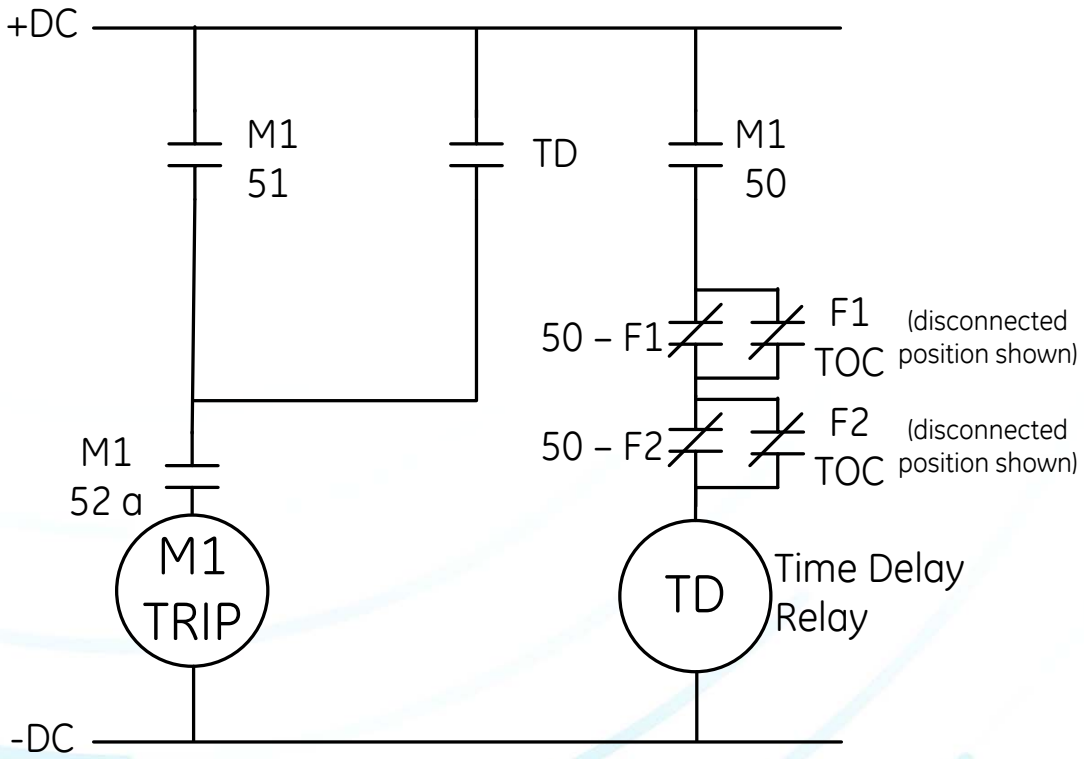


Fails into fast, non-selective (protective) mode.
LV trip units always fail this way!

Fails into slow but selective mode.

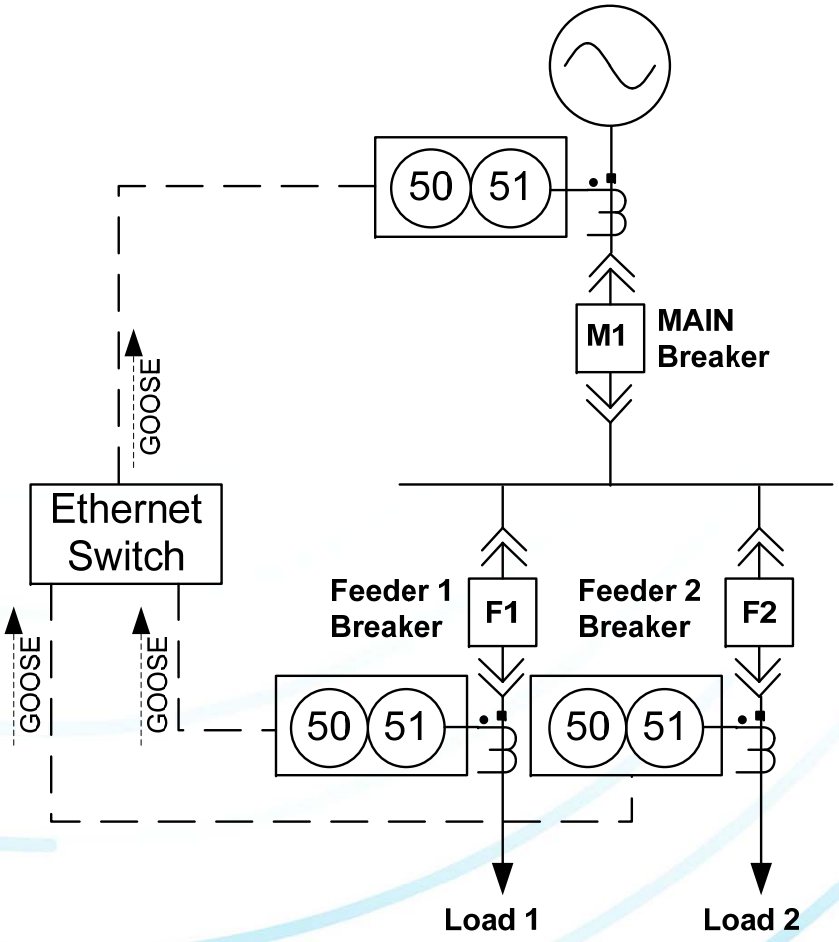


Zone-Selective Interlocking - Hardwiring



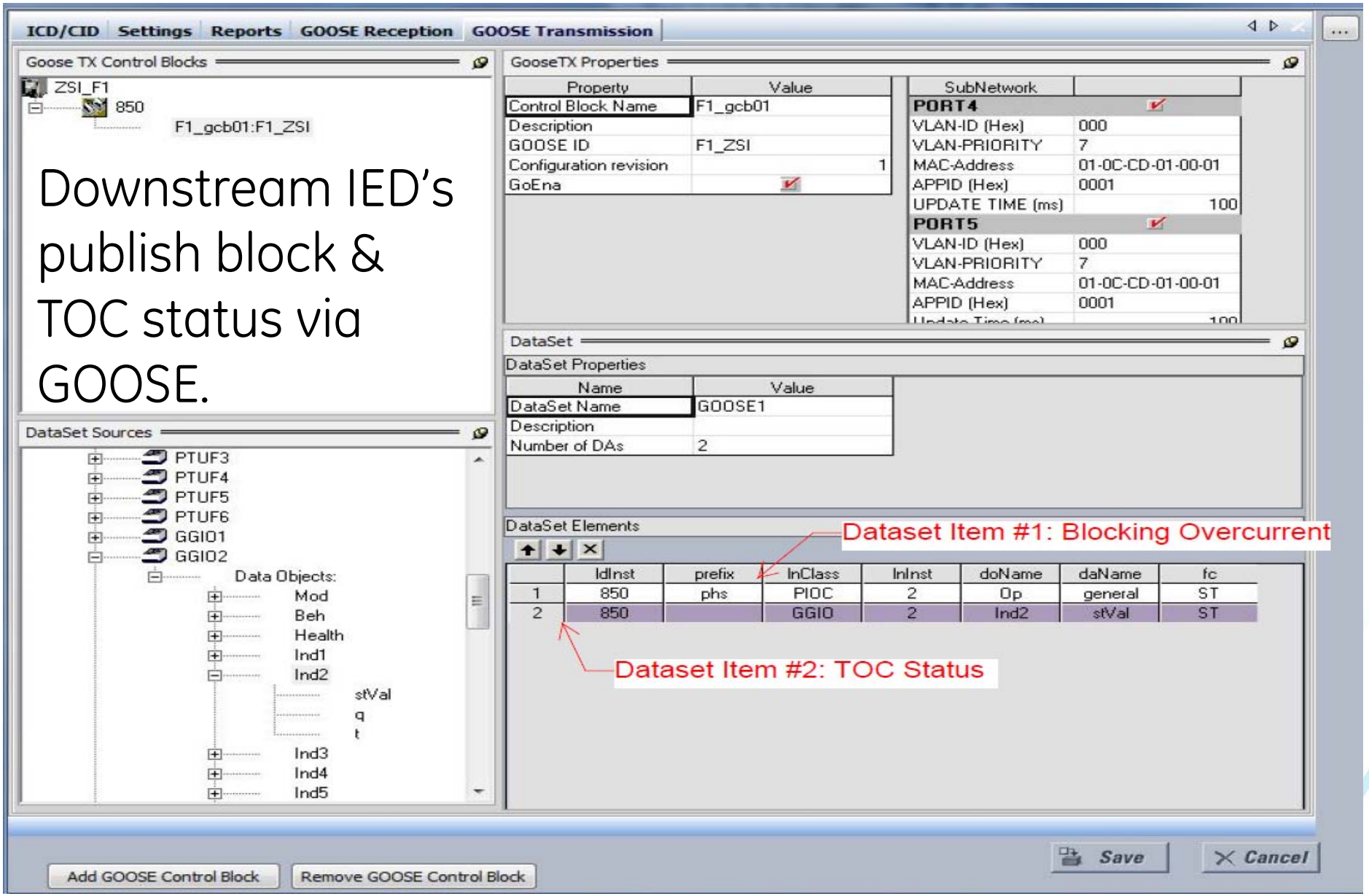
Additional logic can become cumbersome with hardwiring.

Zone-Selective Interlocking - Comms

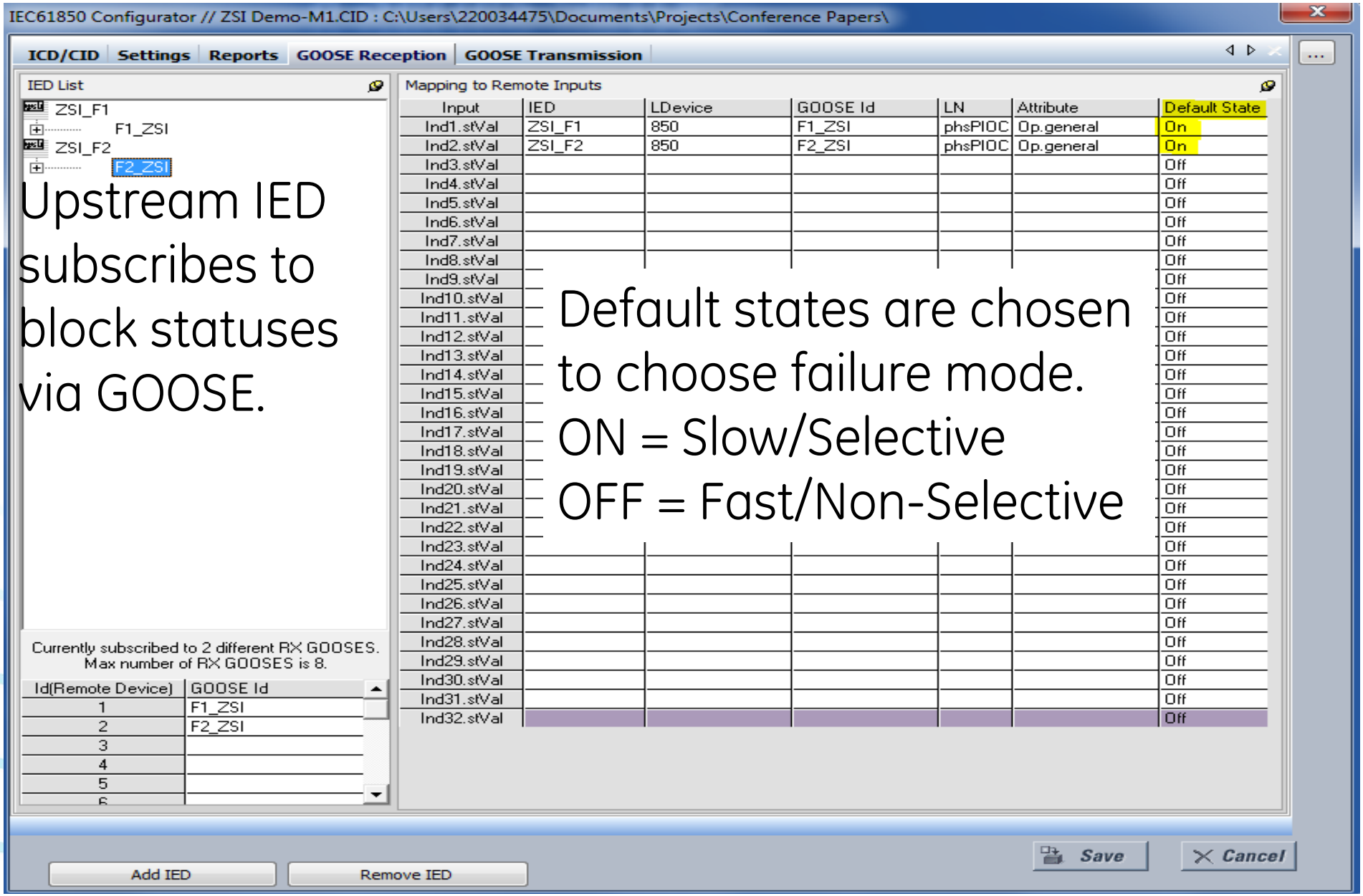


- Communications can be used to simplify wiring.
- Count on 4ms delay for priority GOOSE messages.
- Tripping device has a finite # of devices to which it can subscribe.

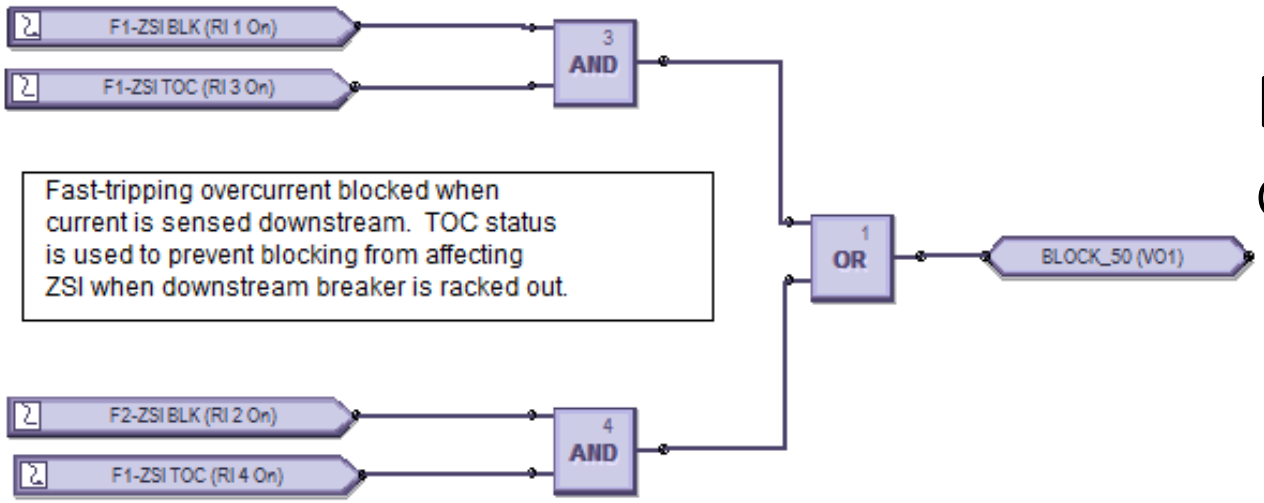
Zone-Selective Interlocking - Comms



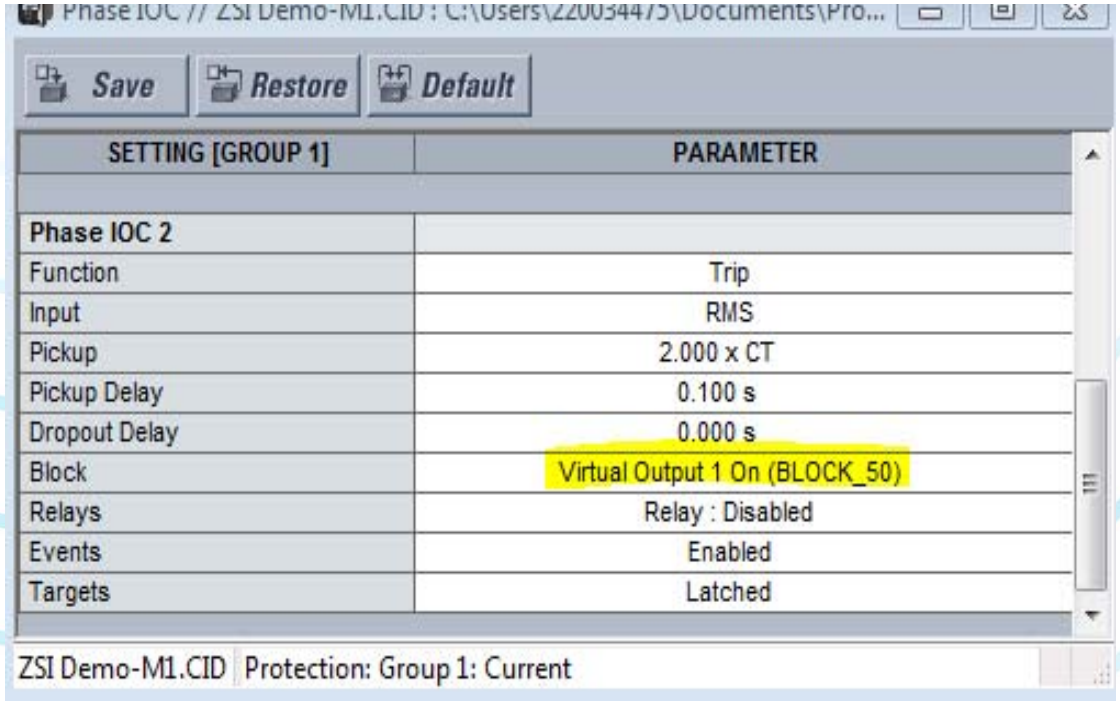
Zone-Selective Interlocking - Comms



Zone-Selective Interlocking - Comms

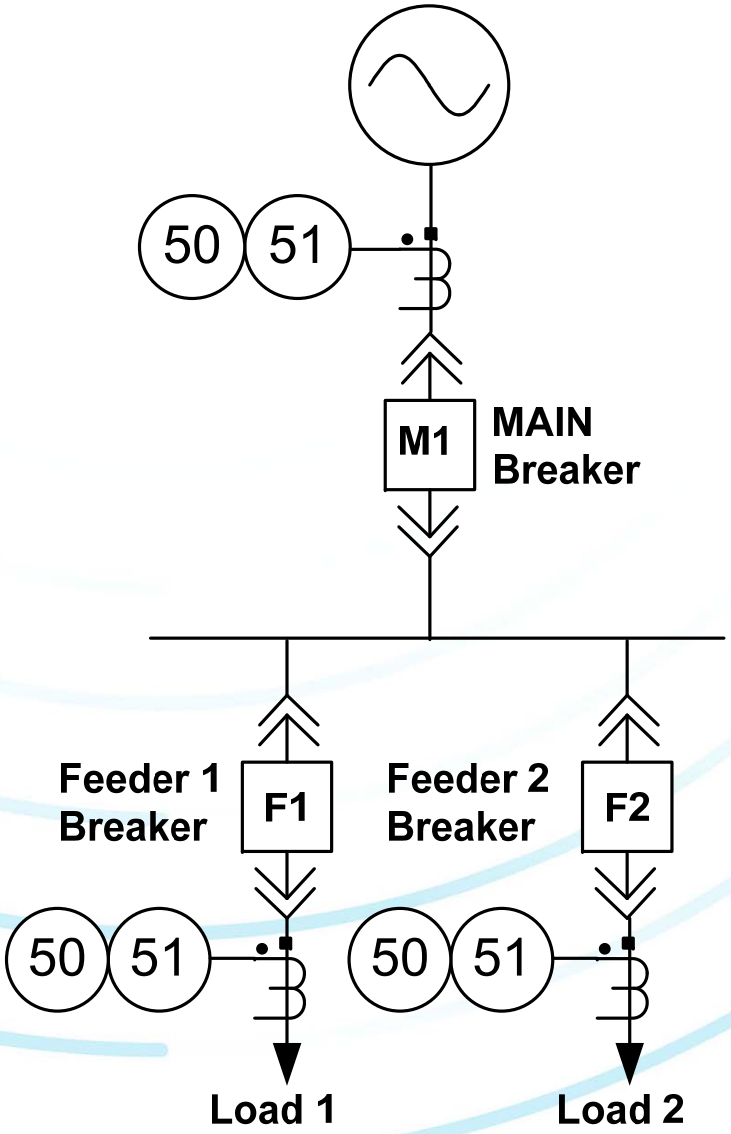


IED logic is created.



Logic is applied to fast-tripping element.

Zone-Selective Interlocking - Pickups



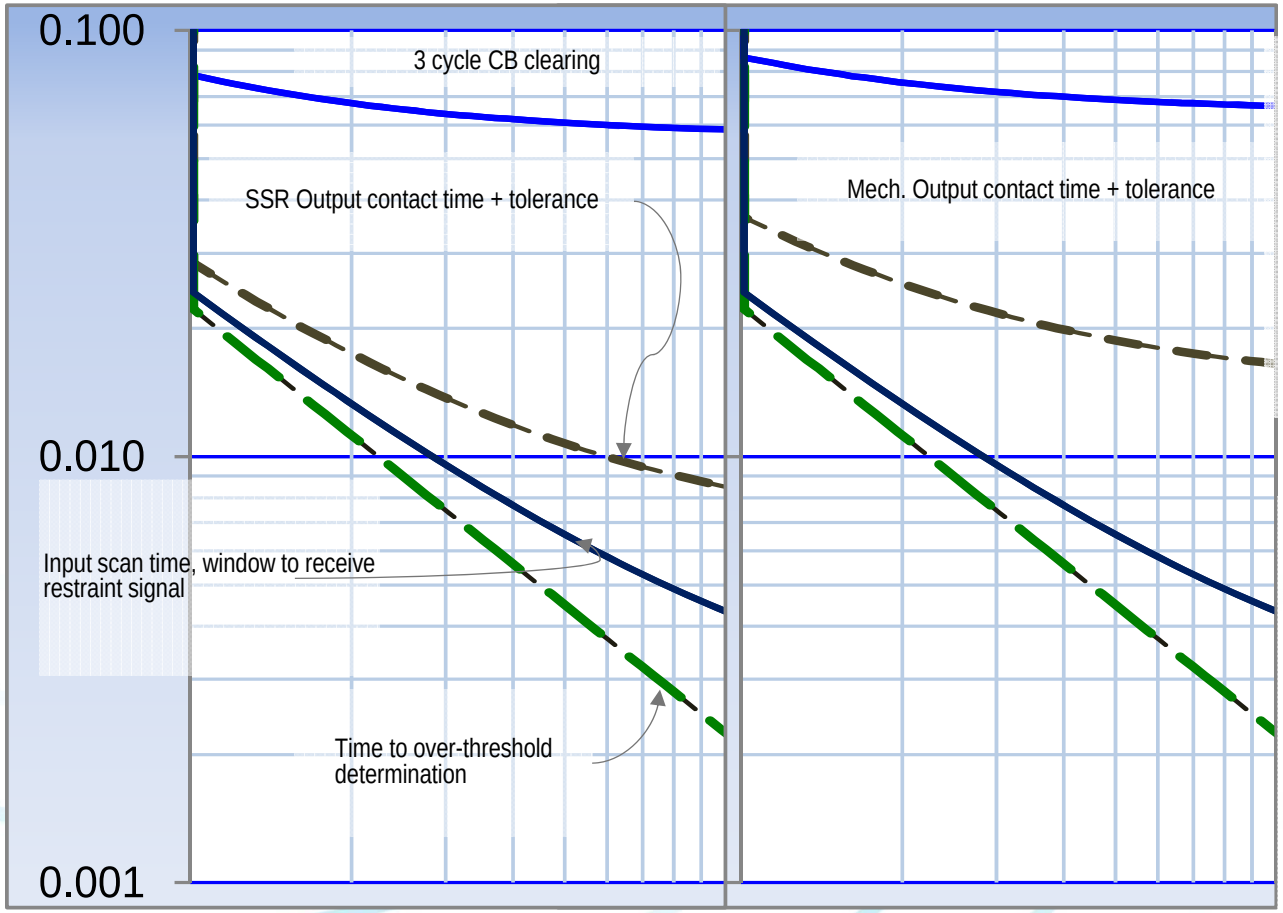
Upstream pickup must not be more sensitive than any downstream pickup. “Tolerance”

Upstream pickup must not pick up for charging current, inrush, etc.

Downstream pickup must not have any delay!

Beware excessively high pickup settings – DSP clamping

Zone-Selective Interlocking - Timing



Left TCC shows plot for the relay's IOC algorithm, 2 mS scan time, SSR output contacts plus tolerance. Right TCC shows mechanical output contacts in lieu of SSR contacts

Tripping can be set with an intentional delay to allow time for restraint signal to be active, OR a relay's inherent inverse time/current characteristic can be used to time-coordinate.

Precise timing requires detailed info from manufacturer.

Even "instantaneous" has an inverse time/current characteristic.

Zone-Selective Interlocking - Timing

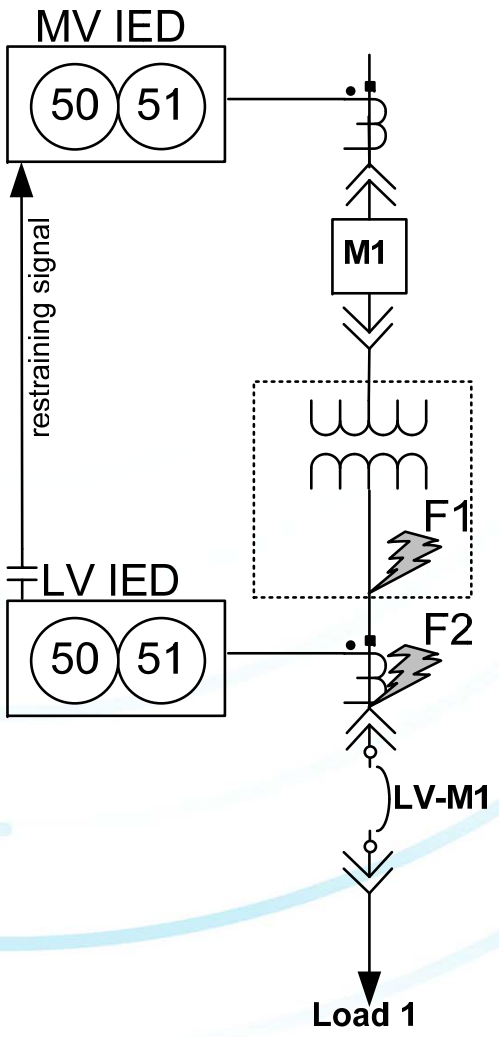
Tripping delay can be set more generally based on readily available manufacturer info.

PHASE/NEUTRAL/GROUND IOC

Current:	Phasor only
Pickup level:	0.020 to 30.000 pu in steps of 0.001
Dropout level:	97 to 98% of pickup
Level accuracy:	
0.1 to 2.0 × CT rating:	±0.5% of reading or ±0.4% of rated (whichever is greater)
> 2.0 × CT rating:	±1.5% of reading
Overreach:	<2%
Pickup delay:	0.00 to 600.00 s in steps of 0.01
Reset delay:	0.00 to 600.00 s in steps of 0.01
Operate time:	<16 ms at 3 × pickup at 60 Hz (Phase/Ground IOC) <20 ms at 3 × pickup at 60 Hz (Neutral IOC)
Timer accuracy:	±3% of operate time or ±1/4 cycle (whichever is greater)

Always weigh the benefits and risks when setting the delay. When reduction of clearing time is of utmost importance, attention to timing detail is extremely important.

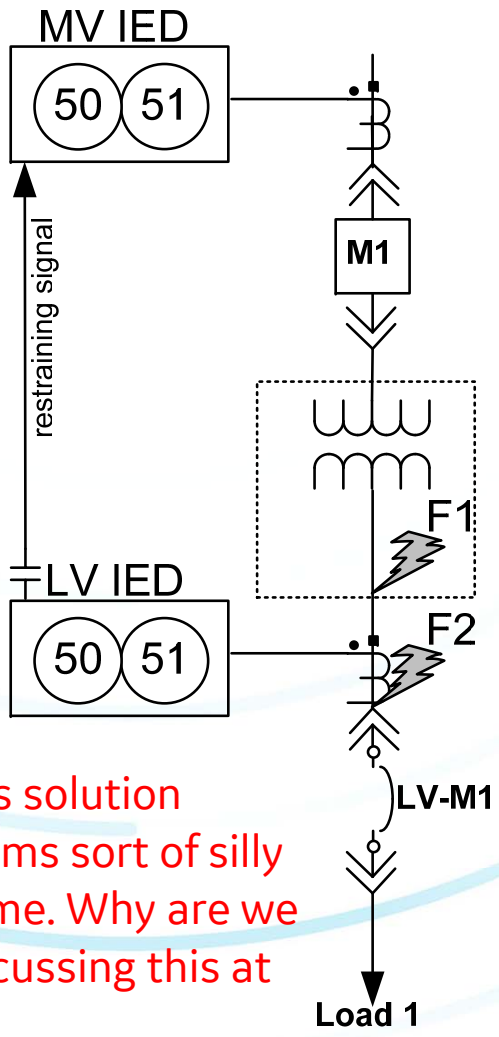
ZSI Challenge #1: Transformer In-zone



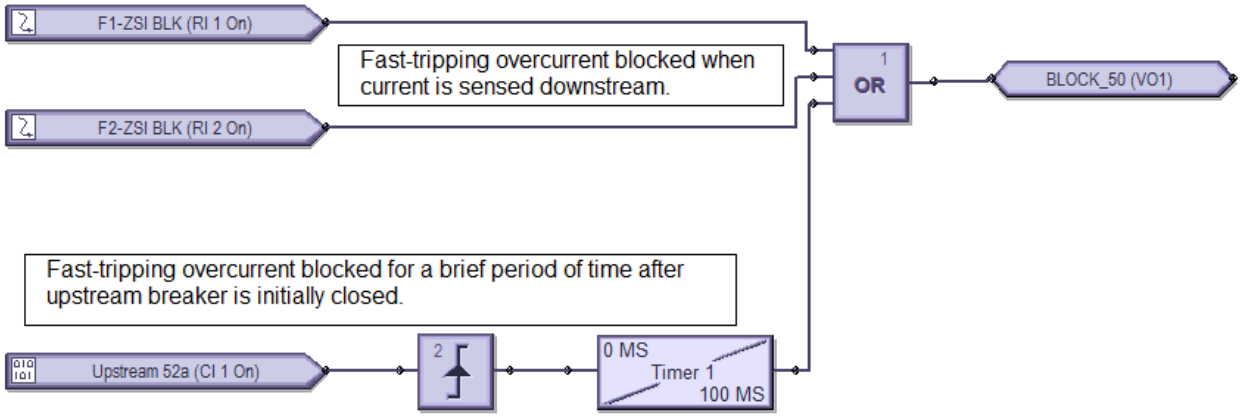
Beware inrush!

This implementation will only expedite tripping for F1. This scheme will not help F2.

ZSI Challenge #1: Transformer In-zone



This solution seems sort of silly to me. Why are we discussing this at all?



MV IED can be blocked for a period of time immediately after energization, but this solution is deficient in two ways:

1) Faults during energization would be slow to clear.

2) Doesn't account for transient recovery inrush.

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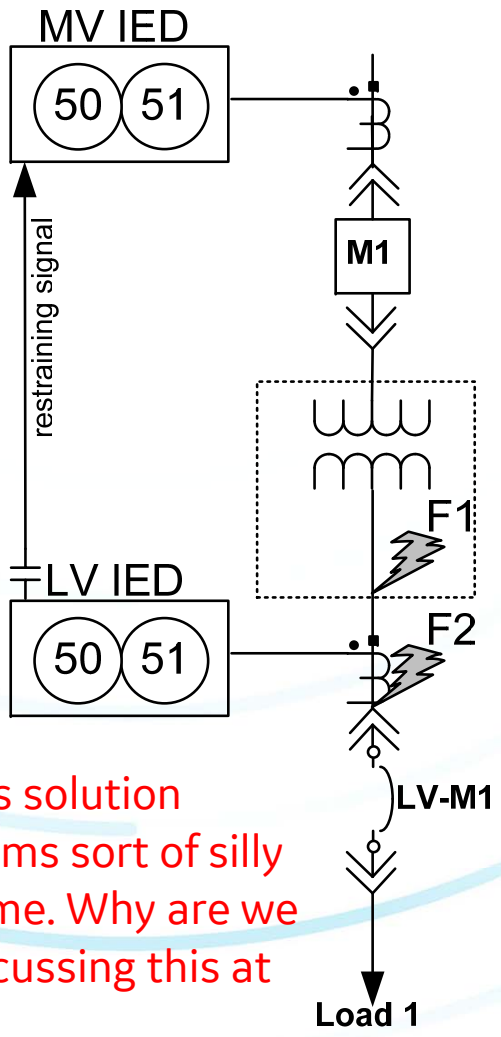

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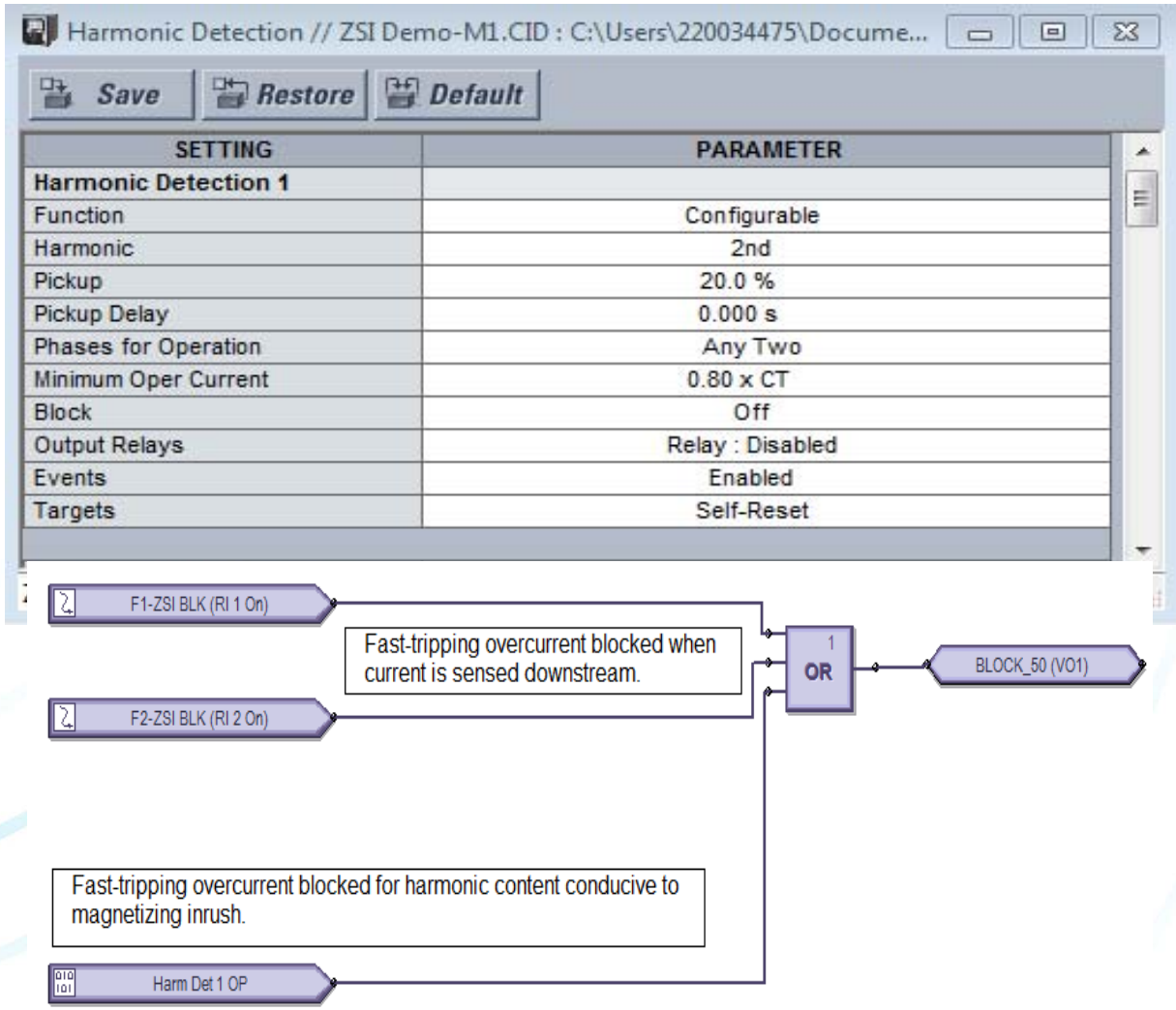

2nd Harmonic detection can be used to address inrush.

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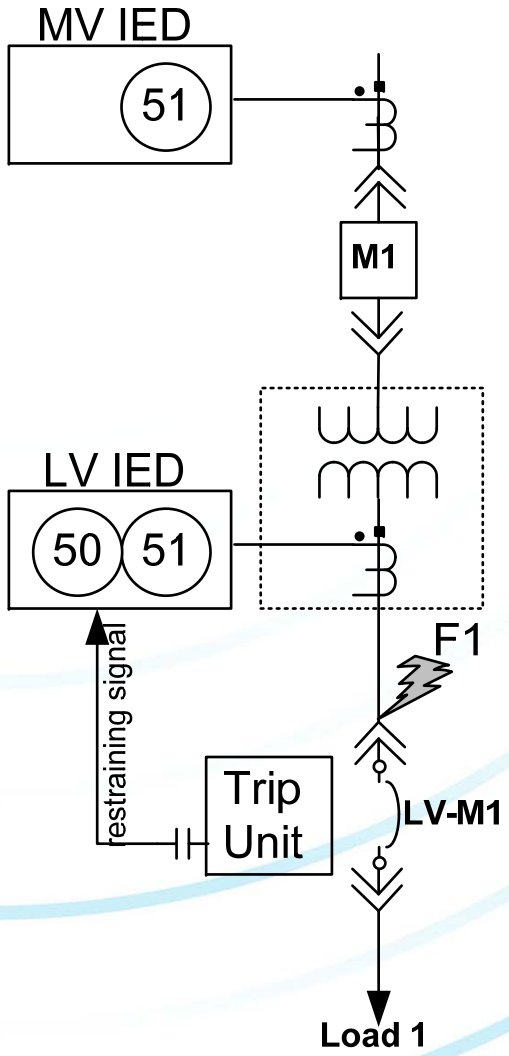
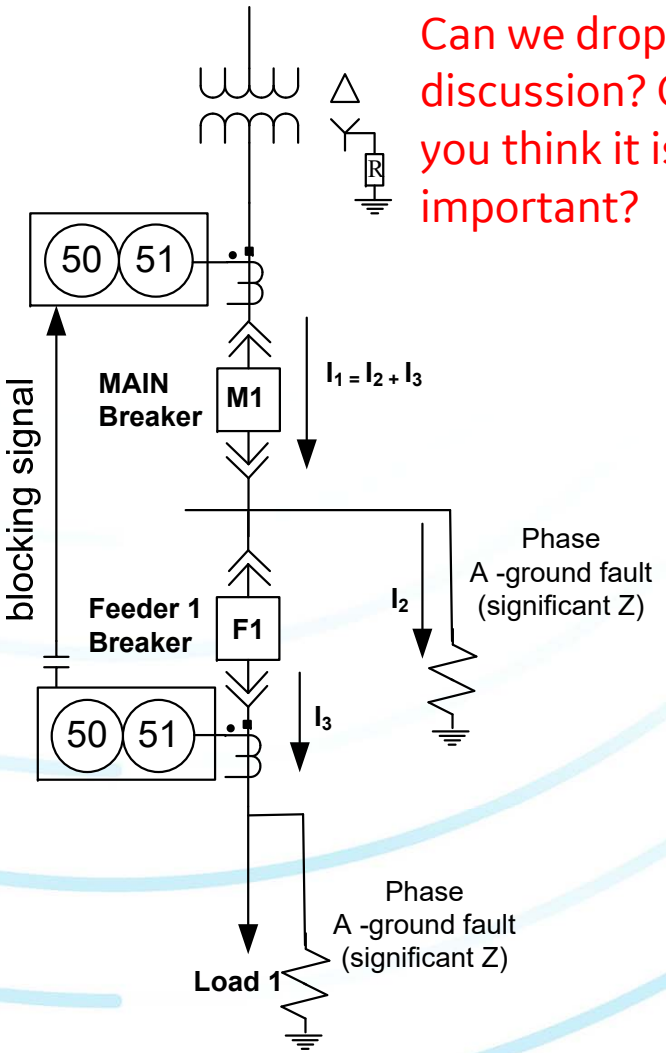


This implementation can expedite tripping for F1.

It is important for the LV IED CT's to be removed from the F1 protected area.

ZSI Challenge #2: Simultaneous Faults



Stress of 1 fault can cause a simultaneous fault.

Under very specific circumstances, the blocking relay would prevent the tripping relay from operating fast.

Normally, fault current would be re-directed into upstream fault so block would be removed.

Conclusions

- ZSI is a longstanding technology that can be used to expedite otherwise slow time-overcurrent protection.
- The scheme can be implemented in many different ways. Consider the failure mode of the scheme.
- Transformer inrush and simultaneous faults offer challenges to ZSI implementation.
- Choose your ZSI timing carefully.

Thank You

Questions?